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# A HARDWARE FAST TRACKER FOR THE ATLAS TRIGGER

*N. Asbah*[1] *on behalf of the ATLAS Collaboration*

DESY, Hamburg, Germany

The trigger system of the ATLAS experiment is designed to reduce the event rate from the LHC nominal bunch crossing at 40 MHz to about 1 kHz, at the design luminosity of $10^{34}$ $\mathrm{cm}^{-2} \cdot \mathrm{s}^{-1}$. After a successful period of data taking from 2010 to early 2013, the LHC already started with much higher instantaneous luminosity. This will increase the load on High Level Trigger system, the second stage of the selection based on software algorithms. More sophisticated algorithms will be needed to achieve higher background rejection while maintaining good efficiency for interesting physics signals. The Fast TracKer (FTK) is part of the ATLAS trigger upgrade project. It is a hardware processor that will provide, at every Level-1 accepted event (100 kHz) and within 100 $\mu$s, full tracking information for tracks with momentum as low as 1 GeV. Providing fast, extensive access to tracking information, with resolution comparable to the offline reconstruction, FTK will help in precise detection of the primary and secondary vertices to ensure robust selections and improve the trigger performance. FTK exploits hardware technologies with massive parallelism, combining Associative Memory ASICs, FPGAs and high-speed communication links.

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## INTRODUCTION

The Large Hadron Collider (LHC) [1] has begun Run II after a two-year shutdown, ready for proton–proton 13-TeV collisions with an instantaneous luminosity that could exceed $10^{34}$ $\mathrm{cm}^{-2} \cdot \mathrm{s}^{-1}$. The number of interactions per collision, mostly forming pile-up (PU) noise, will increase to an average of 40 to 50 collisions per bunch crossing. Run II will bring a higher detector occupancy than previously seen and create a busy and challenging environment for data readout and particle reconstruction. Limited computing resources will require the online data processing to reduce the data output to a manageable level. Sophisticated trigger algorithms will be essential for selecting the events with interesting physics signatures at a high efficiency while rejecting an increasingly large background.

The ATLAS [2] detector will need to make better use of the information received by the silicon detector in order to improve charged particle reconstruction in the heavy pile-up environment. To realize this goal, the ATLAS experiment has decided to include the Fast TracKer (FTK) within its hardware Level-1 (L1) and its software High Level Trigger (HLT) systems [2–4] designed to perform full track reconstruction of the complete granularity of

[1]E-mail: nedaa.asbah@desy.de

the inner detector (ID) [5–7]. FTK will run with an average latency of about 100 $\mu$s and will receive data from 98 million channels for every event passing the L1 trigger at 100 kHz. It will reconstruct trajectories in the silicon detector for charged particles with a transverse momentum above 1 GeV and within $|\eta| < 2.5$[1]. These tracks will be made available for use in the HLT, removing the need for resource heavy, time-consuming tracking in the HLT.

## 1. THE FAST TRACKER ALGORITHMS

The FTK algorithm consists of two main stages. The first stage consists of pattern recognition in the Associative Memory (AM) for quickly and coarsely locating track candidates. Patterns are developed using hits from 8 of the 12 detector layers; 2 of the 4 pixel layers and 6 of the 8 axial and stereo channels from the Silicon Strip Detector (SCT). Potential patterns are pre-calculated using Monte Carlo simulation and stored for reference in a Pattern Bank. Hits in each event are compared with all the patterns in the Pattern Bank and track candidate are found, called roads.

The second stage consists of the Track Fitter for fitting the full-resolution hits in each candidate road to determine the optimal track parameters and reject false pattern matches. Track parameters are evaluated from the full-resolution hits using a linear combination of the following form:

$$p_i = \Sigma_j a_{i,j} x_j + b_i,$$

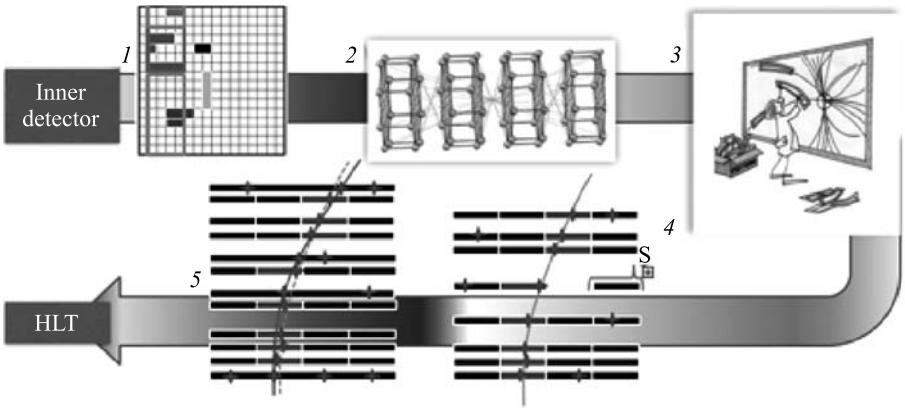


Fig. 1. The main steps of the FTK algorithm; *1* — data is received from the inner detector and clusters are found; *2* — clusters are geometrically organized in overlapping towers; *3* — candidates are found using 8 detector layers; *4* — a first track fit is performed; *5* — refine fit using hits from the previously ignored detector layers [9]. More details about the different fitting stages are in the following section

[1]ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the center of the detector and the $z$ axis coinciding with the axis of the beam pipe. The $x$ axis points from the IP to the center of the LHC ring, and the $y$ axis points upward. Cylindrical coordinates $(r, \phi)$ are used in the transverse plane, $\phi$ being the azimuthal angle around the beam pipe. The pseudorapidity is defined in terms of the polar angle $\theta$ as $\eta = -\ln(\tan(\theta/2))$.

where $p_i$ is either a helix parameter or a term used in the $\chi^2$ fit. The parameters $a_{i,j}$ and $b_i$ are pre-calculated constants. Each road is attributed to a "sector" in which fixed $a_{i,j}$ and $b_i$ are valid. The $x_j$ are the hit coordinates in the silicon layers.

In the complete FTK system there are about $10^9$ predefined patterns, organized in about $10^6$ distinct sectors. The FTK main algorithms are summarized in Fig. 1 [8], and more details are explained in the following section. All of these steps are done quickly in custom integrated circuits and modern FPGAs. Rates of 1 track fit/ns are achieved.

## 2. THE FTK HARDWARE COMPONENTS

The FTK algorithms are implemented in electronics boards using VME and ATCA standards. The final system will have approximately 2000 FPGAs and 8000 AM custom ASICs. The system uses 32 Data Formatter (DF) boards, 128 associative memory boards serial link processors (AMB or AMBSLP) and auxiliary cards (AUX), 32 second stage boards (SSB), and 2 FTK to Level-2 interface cards (FLIC). A detailed description of each board is presented in the following [8].

The FTK system starts with the DF boards and embedded FTK input mezzanine (FTK_IM) boards (Fig. 2) which receive pixel and silicon strip data transmitted using dual-output high-speed optical links (SFP using CERN's S-Link protocol [12]). The FTK_IM receives data from 4 S-Links for a total traffic of 500 Gbps between the detector front end and FTK. The FTK_IM performs dedicated cluster-finding algorithms on pixel hits. More details on clustering can be found in [10]. Then the DF reorganizes the data, combining hits into $\eta$–$\varphi$ towers, and sends them to the next stages where they can be processed.

Fig. 2. The FTK Input Mezzanine Cards, four of which attach to the Data Formatter through the FMC connector

The core of the FTK system is composed of the AM board and AUX cards (Fig. 3), where the pattern matching and the first stage fitting is performed, respectively. The data are organized by layers and sent to the AUX by the DF, where two algorithms are performed; the Data Organizer (DO) and the Track Fitter (TF). The DO organizes all the clusters according to a coarse resolution position identifier and produces super strips (SSs). Then the SSs are sent to the AM board for the pattern matching. The AM boards hold preloaded patterns corresponding to the 8 silicon layers. The SSs from the AUX are compared to the AM patterns and the resulting roads are sent to the TF. Finally, the TF builds and fits all combinations of clusters in a road, sending only candidate tracks with acceptable $\chi^2$ values

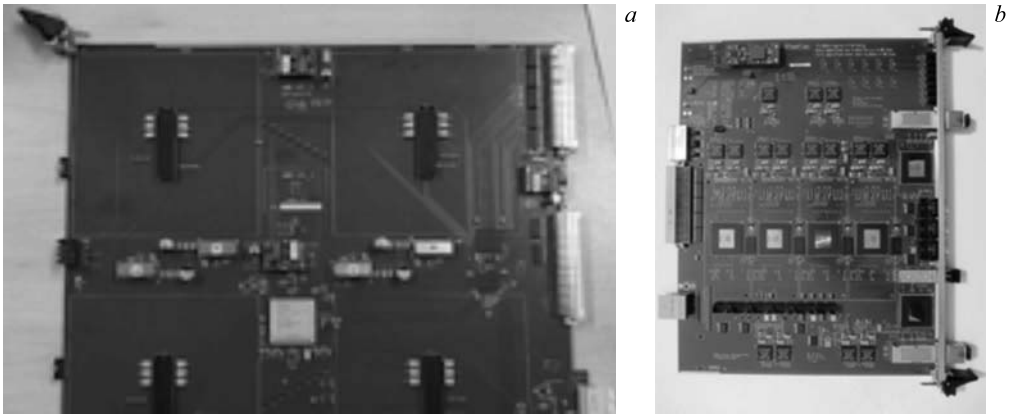


Fig. 3. The second prototype of the AMB board (*a*) and the second prototype of the AUX board (*b*). The AMB contains 63 AMchips divided into 4 mezzanines; 16 chips per mezzanine

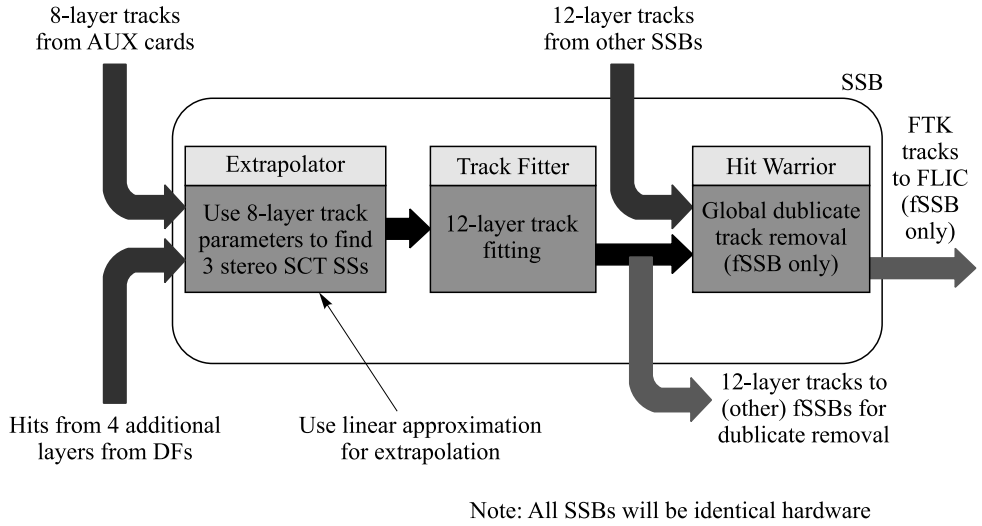


Fig. 4. The SSB functional diagram summarizing the primary functions of the SSB [8]

to the SSB for further processing. Duplicated tracks are removed in the AUX Hit Warrior (HW) algorithm.

The SSB receives the candidate roads passing the first stage fits and supplements them with the cluster centroids from the 4 unused layers from the DF, and additional refinement of the tracks is performed. The complete SSB functional diagram is shown in Fig. 4. Duplicate tracks are removed in the SSB before being sent to the final stage of the FTK system, the FLIC board. The final tracks from the SSB are organized and reformatted by the FLIC and sent to the High Level Trigger ROSs using the standard ATLAS protocols event format [8].

## 3. FTK EXPECTED PERFORMANCE

To better tune the FTK algorithms and to improve its performance within the HLT selection, a great deal of effort has been dedicated towards simulation studies. The tracking performance has been studied in single particle MC samples, exploring the efficiency for finding particles (muons, pions, etc.) as well as the performance of the offline track reconstruction (Fig. 5). Overall, the FTK track finding efficiency is of comparable quality to offline with an efficiency of about 95% and a fake rate of 5% at an overwhelming 70 proton–proton interactions per bunch crossing, the expected LHC operating condition for Run III [8].

The role of FTK is to perform tracking as a first stage of the HLT. Algorithms are under development to handle complicated backgrounds without rejecting interesting physics, especially the typically low efficiency signals such as hadronically decaying $\tau$'s and $b$-hadron jets ($b$-jets). Figure 6 shows an improvement in the trigger efficiency for $\tau$'s from Higgs at

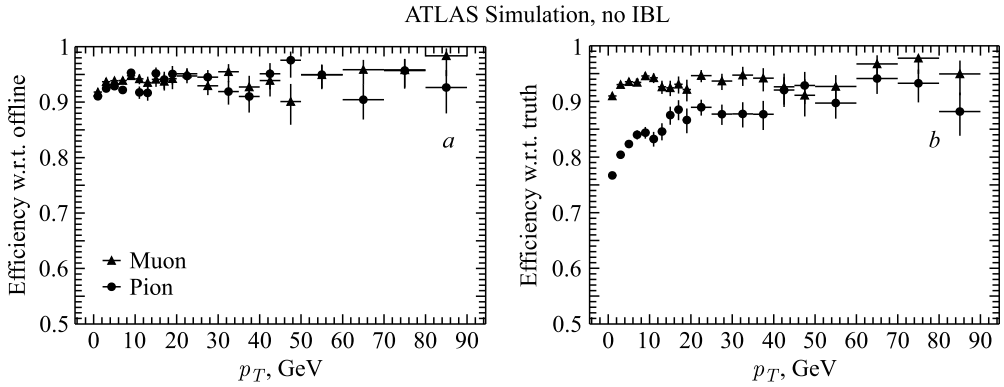


Fig. 5. FTK efficiency versus $p_T$ for muons and pions samples with respect to offline track reconstruction ($a$), and the absolute efficiency ($b$) [8]

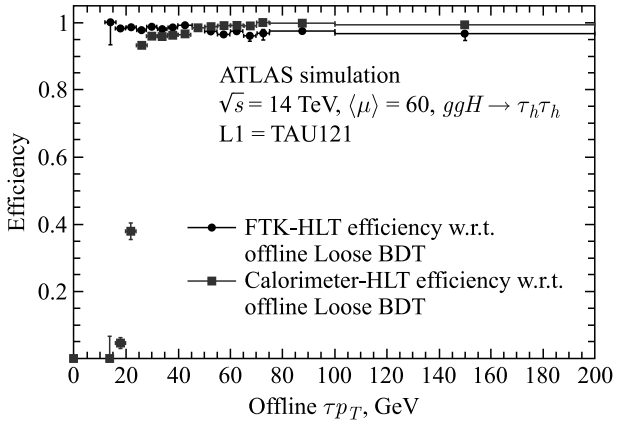


Fig. 6. Comparison between HLT efficiency using FTK reconstructed tracks (circle) and that using only calorimeter algorithms (square) with respect to offline reconstructed taus in the $\mathrm{H} \to \tau\tau$ at $\mathrm{PU} = 60$ [11]

low momentum when using optimized algorithms with FTK tracks. More detailed studies of the FTK performance can be found in [8].

## 4. COMMISSIONING WITHIN THE ATLAS DETECTOR

Development of FTK is on track with the original schedule for commissioning within ATLAS. Most of the hardware is ready for production. A demonstrator system, including at least one board from each step of the FTK system, is planned for commissioning near the end of the 2015 data taking period. The FTK group is aiming to have a fully working system to reconstruct tracks in the full barrel region in early 2016 and expanding coverage to the whole inner detector six months later.

## CONCLUSIONS

The ATLAS FTK system is designed to perform global track reconstruction at the full Level-1 trigger rate. Using a massively parallel configuration of Associative Memories, FTK will reconstruct tracks within 100 $\mu$s at the beginning of the HLT, allowing extended tracking capabilities while freeing the precious HLT resources currently used in track finding. Full event tracking is a powerful tool to reduce trigger sensitivity to pileup, with a precise reconstruction of collision vertices, and to increase efficiency on selecting taus and $b$-jets. The FTK track quality and efficiency are compatible with the offline performance. Most of the hardware is ready for production and a first complete slice of the system will be ready for testing during the 2016 ATLAS data collection.

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