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PHASE-I TRIGGER READOUT ELECTRONICS UPGRADE OF THE ATLAS LIQUID-ARGON CALORIMETERS

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This article gives an overview of the Phase-I Upgrade of the ATLAS LAr Calorimeter Trigger Readout. The design of custom developed hardware for fast real-time data processing and transfer is presented. Performance results from the prototype boards operated in the demonstrator system, first measurements of noise behavior and responses on the test pulses to the demonstrator system are shown.

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INTRODUCTION

The Large Hadron Collider (LHC) is foreseen to be upgraded during the shut-down period of December 2018 – February 2021 for improvement of the instantaneous luminosity. For improving the selectivity of electromagnetic (EM) and τ objects, the resolution of jets and E_T^{miss} trigger signatures, and the discrimination power against background emerging from pileup, the trigger readout of the ATLAS LAr Calorimeters will be upgraded [1]. The granularity will be increased 10 times. This is called "Phase-I Upgrade". The legacy Trigger Tower readout and the new Super Cell readout are described in Fig. 1 [2]. As shown in Fig. 2, the legacy readout path and the new readout path will be prepared in parallel in order to keep the legacy trigger path as a fallback.

1. NEW CUSTOM DEVELOPED HARDWARE FOR SUPER CELL

The new readout path consists of new custom developed hardware for the Super Cell Readout to achieve fast real-time data processing and transfer (Fig. 2). In this section, four new components, a new baseplane, a new layer sum board, the LAr Trigger Digitizer Board (LTDB), and the LAr Digital Processing System (LDPS), are overviewed.

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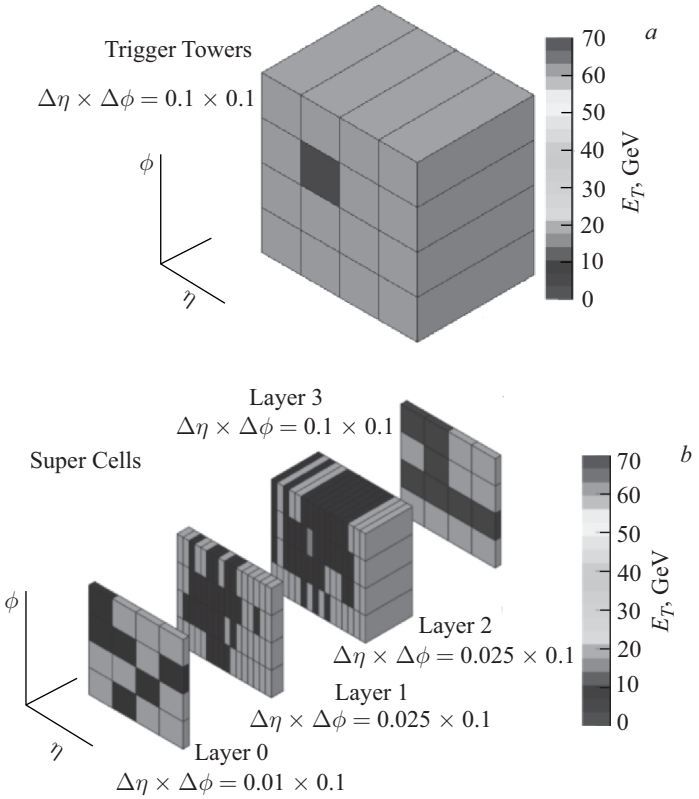

Fig. 1. The energy depositions of an electron which carries energy of 70 GeV are illustrated for two cases. *a*) Trigger Tower readout, which sums the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. *b*) Super Cell readout, which provides information for each calorimeter layer for the full η range of the calorimeter, and finer segmentation ($\Delta\eta \times \Delta\phi = 0.025 \times 0.1$) in the front and middle layers

1.1. New Layer Sum Board. The current layer sum board (LSB) provides summation of analog signals of the elementary LAr Calorimeter cells over a range of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ for a given layer of the calorimeter. During the Phase-I Upgrade, the new LSB processes 4 times finer segments ($\Delta\eta \times \Delta\phi = 0.025 \times 0.1$) for the summation in the Front and Middle layers. The new LSBs are mounted on the Front-End Board (see the upper left side of Fig. 2).

1.2. New Baseplane. In order to allocate new slot for LTDB and to route the analog signal from Front-End Boards, the baseplane is replaced. In this configuration, a much larger number of signals are transferred through the baseplane. It also routes the legacy trigger signals to the Tower Builder Board, as is done by the current baseplane.

1.3. LAr Trigger Digitizer Board. Primary role of LTDB is to digitize the Super Cell signals from the new LSB. The 40 MHz sampling digitization is realized with custom developed 12-bit SAR ADC in 130 nm CMOS technology, which has a good level of radiation tolerance (see Fig. 3).

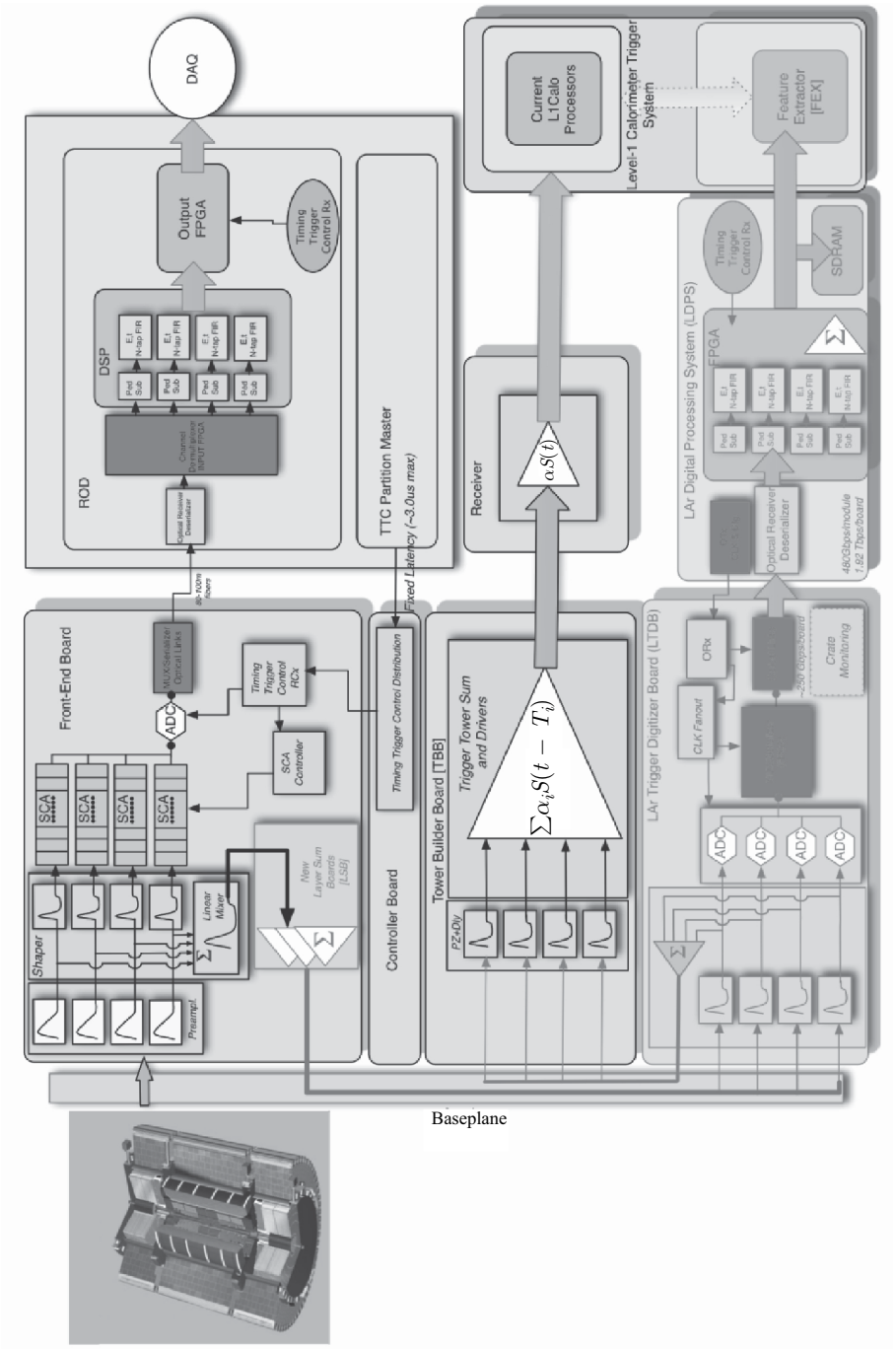

Fig. 2. Schematic diagram of the architecture of the readout electronics after the Phase-I Upgrade

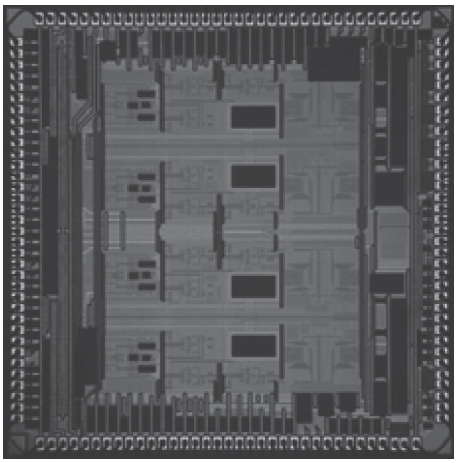

Fig. 3. Chip die of the prototype of custom ADC (NEVIS13) [3]

The other role is to transmit the digitized signal to the LDPS. LOCx2 serializer and LOCld optical driver [4] are developed to perform the data transfer at 5.44 Gb/s per fibre; 40 fibers are used in total. Each of the 124 LTDBs handles up to 320 Super Cell channels.

1.4. LAr Digital Processing System. There are three roles assigned to the LDPS. First, the LDPS receives the digitized data at a total rate of 25 Tb/s. Second, the LDPS reconstructs

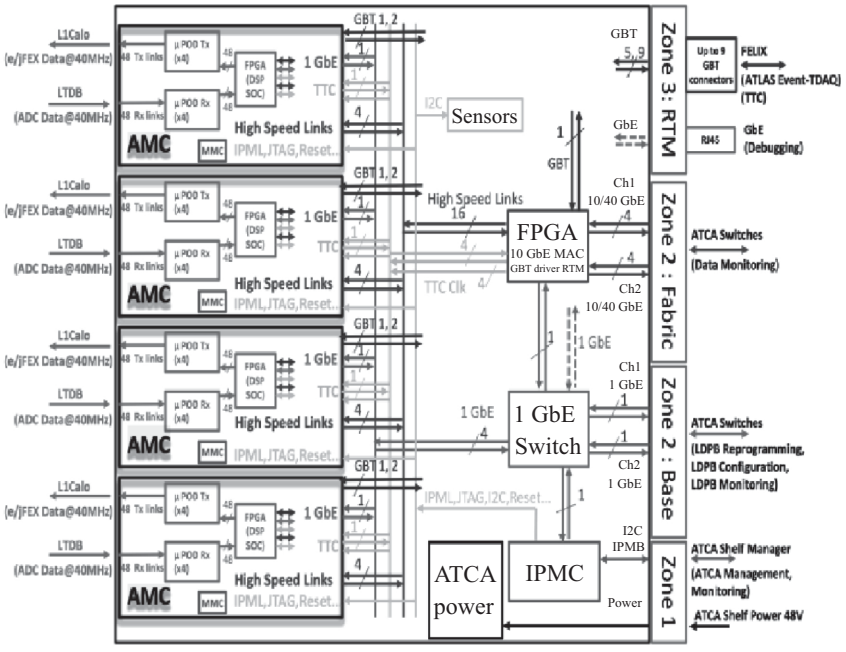

Fig. 4. Schematic diagram of LDPB, which contains four AMCs (see Fig. 5)

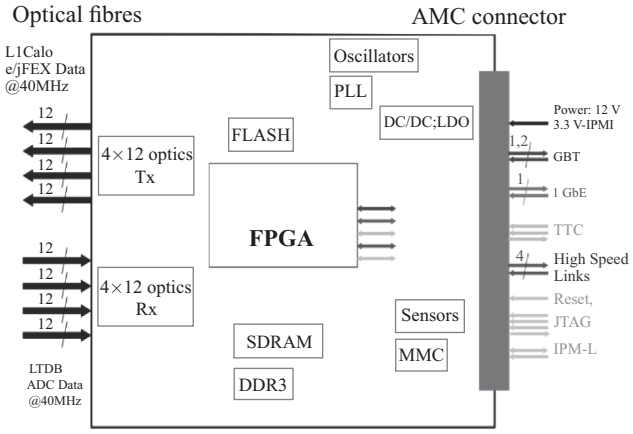

Fig. 5. Schematic diagram of an AMC, with an ALTERA Arria-10 FPGA in the center

transverse energies of each Super Cell and also calculates energy sums in real time. Finally, the LDPS transmits data containing the transverse energy information to the Level-1 trigger processors. For achieving these roles, LDPS in design consists of 32 ATCA carrier blades, LDPB (see Fig. 4), which carry 4 Advanced Mezzanine Cards (AMC) each (see Fig. 5). On the AMCs, precise energy reconstruction, pileup suppression, and identification of the correct bunch crossing time are performed. Each AMC carries one ALTERA Arria-10 FPGA for the real-time processing which handles 320 Super Cells at maximum.

2. PHASE-I DEMONSTRATOR SYSTEM

For developing hardware, obtaining the installation experience, and testing and validating the performance of the Super Cell, a Demonstrator system has been integrated in the ATLAS detector in Summer 2014. LTDB Demonstrators are installed in one of front-end crates as shown in Fig. 2. The LTDB Demonstrator reads out Super Cells for the region of a barrel part of the LAr Calorimeter, $1.767 < \phi < 2.160$, $0 < \eta < 1.4$, and operates in parallel to the regular ATLAS data taking during the LHC Run 2. Figure 6 shows two types of demonstrators, developed by BNL and LAL/Saclay. The BNL LTDB uses analog mezzanine and digital main board. The LAL/Saclay LTDB has a design with opposite configuration, digital mezzanine and analog main board. A commercial product, TI ADS5272, is chosen as ADC in both LTDBs. The digitized data is transmitted to the pre-prototype LDPB, developed by LAPP (see Fig. 7), which have been installed in USA15 (Backend part of ATLAS). The LDPB is designed along with a commercial Advanced Telecommunications Computing Architecture (ATCA) system. Its core components are ALTERA ® Stratix IV FPGAs. The two front FPGAs receive the digitized data and format them in ATLAS RAW Event Format. The formatted event data is transferred through the back FPGA, via ATCA fabric interface with IPbus and Internet Control Message Protocol (ICMP). These three FPGAs are interconnected via XAUI.

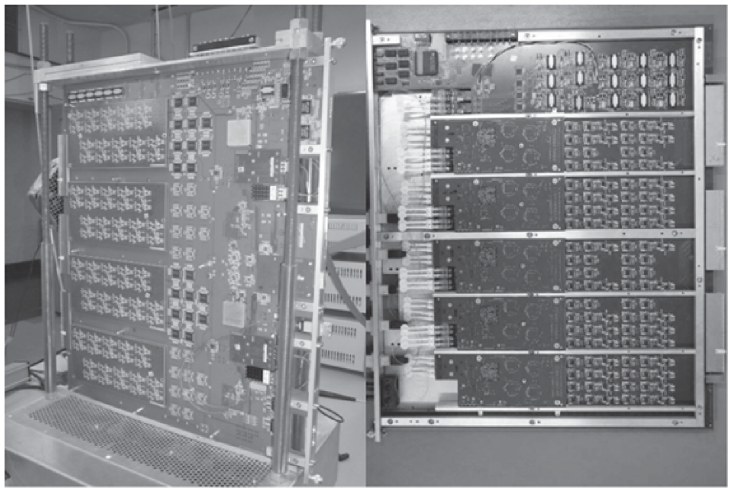

Fig. 6. The two types of LTDB demonstrators, developed by BNL (left) and LAL/Saclay (right), respectively

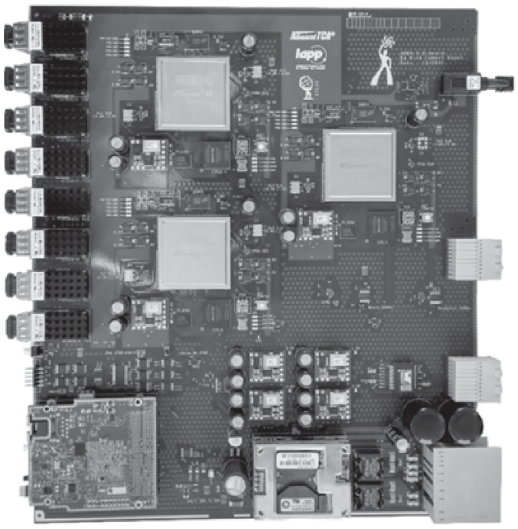

Fig. 7. The pre-prototype LDPB developed in LAPP

3. PERFORMANCE RESULTS OF THE PHASE-I DEMONSTRATOR SYSTEM

This section shows the results of measurement on the demonstrator system [5]. First, the performance of the legacy readout is discussed, followed by the demonstrator readout.

3.1. Measurements with the Legacy Readout. The purpose of measurements with the legacy readout is for assuring that the LTDB demonstrator does not degrade the performance of the energy measurement for the current physics run. First, using a calibration system, we

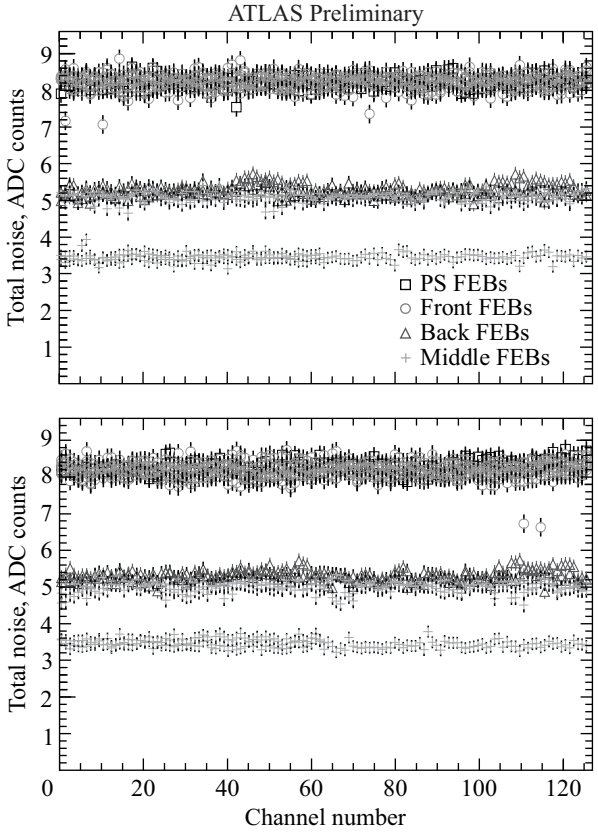

Fig. 8. The RMS of pedestal run for channels of the Front-End Boards in the demonstrator crate (*a*) and same sets in the neighboring crate (*b*). There are 28 Front-End Boards per crate, each has 128 channels. The noise levels of the boards vary because different capacitances and gains are applied to their respective cells [5]

confirmed that there is no dead channel and adjusted the gain level in each channel. The total noise and coherent noise fraction of front-end boards were measured with the legacy readout. Figures 8 and 9 are a comparison of the total noise and the coherent noise fraction of front-end boards for the demonstrator crate and for neighboring crates. The noise level of the demonstrator crate is consistent with that of neighboring crates. Figure 10 shows the total noise on the Trigger Tower readout. The observed noise level is consistent with the current system.

3.2. Measurements with the Demonstrator Readout. We have evaluated the prototype LTDB performance in terms of noise, pulse and linearity. Figure 11 shows the RMS of the pedestal run in ADC counts for the LTDB Demonstrator as function of η. The noise level is as expected between 100 and 250 MeV per Super Cell. Figure 12 shows the responses of four super cells (one from each layer) from the LTDB Demonstrator to injected calibration pulses (DAC = 1000 to each LAr cell). The size and shape of pulses are as expected and vary due to different detector and electronics properties. Figure 13 shows pulse shapes of

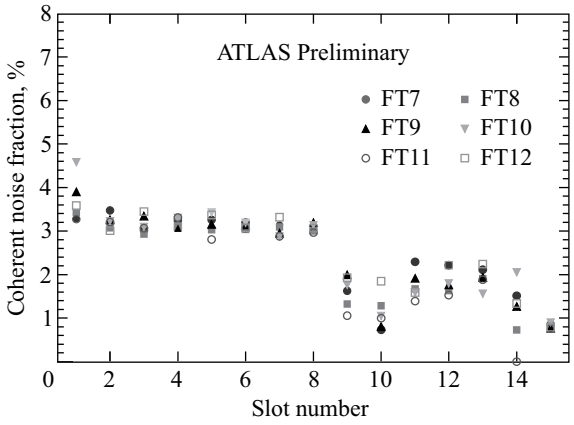

Fig. 9. The fraction of coherent noise per readout channel (Coherent Noise Fraction, CNF) for feedthroughs (FT) 7–12 on the calorimeter. FT9 and 10 belong to the demonstrator crate. FT7, 8, 11, and 12 belong to the neighbor crate. The board in the first slot reads out the presampler, the boards in the following seven slots read out the front layer, the next two boards the back layer and the last four boards the middle layer of the calorimeter. The last entry is the CNF of the whole half crate. The coherent noise fraction was calculated according to the following equation: $\rho_{\mathrm{CNF}} = \dfrac{\sqrt{\sigma^2_{\sum\limits_{i\in A}} - N_{i\in A}\langle\sigma^2_{i\in A}\rangle}}{N_{i\in A}\langle\sigma_{i\in A}\rangle}$, where A is a set of channels, $N_{i\in A}$ is the number of channels belonging to A [5]

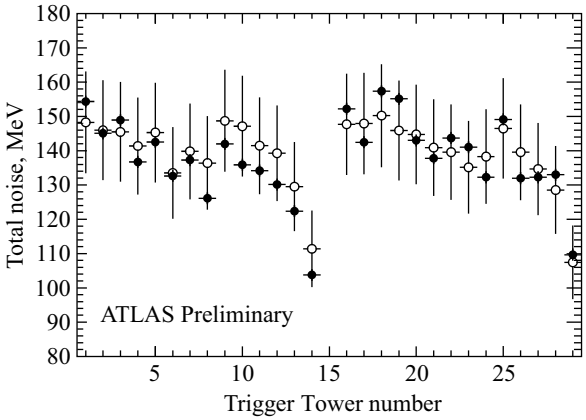

Fig. 10. The total noise in the trigger readout path on the demonstrator system in transverse energy in MeV. Trigger Tower 1–14 correspond to 0 to 1.4 in η and 16–29 are the same in η, but adjacent in ϕ. The values represented by the full circles were measured by a spectrum analyzer, and the values shown in open circles were measured with Flash ADCs [5]

a super cell from the demonstrator for injected calibration pulses with different amplitudes. The size and shape of pulses are as expected and show good linearity up to DAC = 8000, while beyond, analog saturation occurs upstream of the demonstrator board as expected by

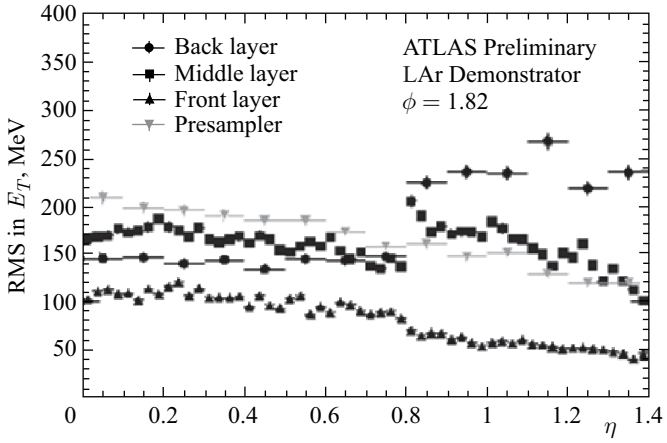

Fig. 11. Pseudorapidity dependence of the RMS of the transverse energy of the Super Cells from the demonstrator setup without beam. The jump seen at $\eta = 0.8$ reflects the change of absorber thickness, electrodes and calibration resistors. The noise level is as expected between 100 and 250 MeV per super cell [5]

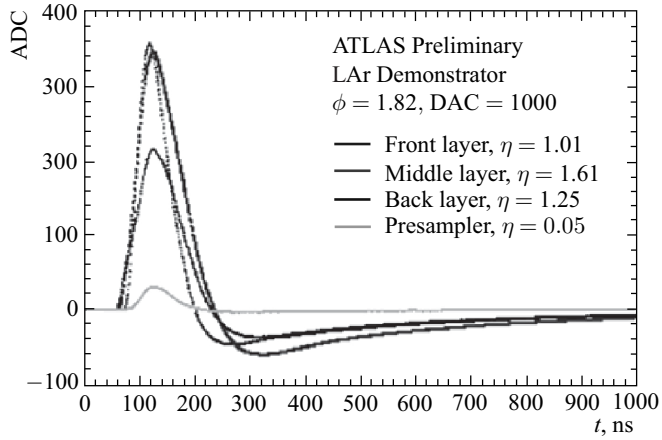

Fig. 12. Responses of four super cells (one from each layer) from LTDB Demonstrator to injected calibration pulses (DAC = 1000 to each LAr cell) [5]

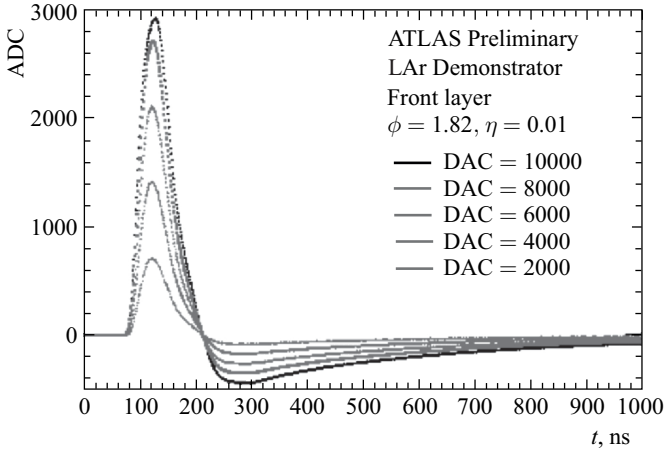

Fig. 13. Pulse shapes of a super cell from the demonstrator for injected calibration pulses with different amplitudes [5]

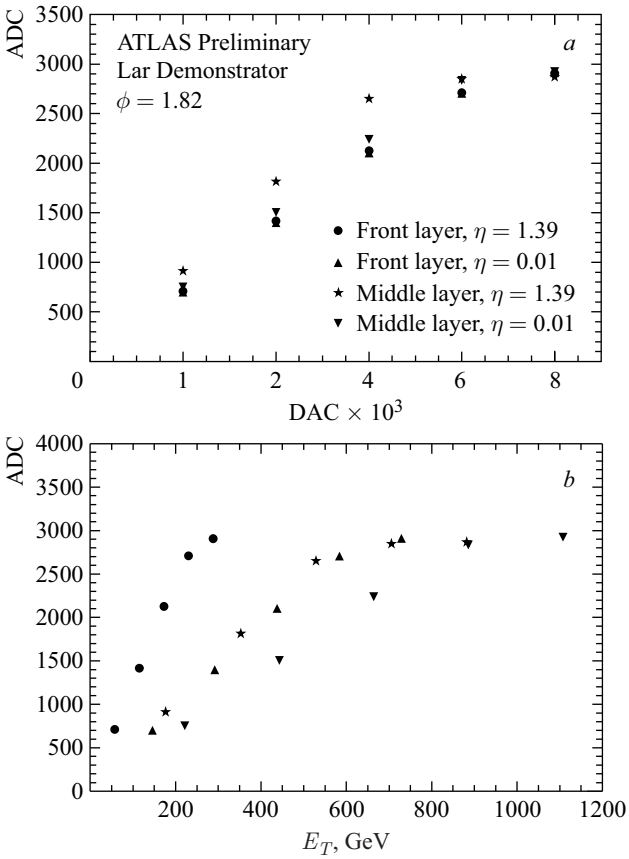

Fig. 14. Pulse maximum in ADC counts for four different super cells from the demonstrator for injected calibration pulses amplitude in DAC (*a*) and transverse energy (*b*) [5]

the design. In Fig. 14, the pulse maximum in ADC counts for four different super cells from the demonstrator as function of the amplitude of injected calibration pulse in DAC (*a*) and transverse energy (*b*) are shown. The pulse shapes shown in Fig. 13 correspond to blue up triangles in Fig. 14. In Fig. 14, *b*, one can observe that the linearity is kept up to sufficiently large values of E_T.

CONCLUSIONS

During Phase-I Upgrade, the trigger readout of ATLAS LAr calorimeter will be upgraded from Trigger Towers to Super Cells. The Super Cell based readout provides higher granularity information to the ATLAS trigger system which can realize high signal efficiency with keeping trigger rate low under high luminosity environment. For achieving the Super Cell readout, custom developed hardware will be installed. The designs on two important hardware of this upgrade, the LAr Trigger Digitizer Board (LTDB) and the LAr Digital Processing System (LDPS), have been presented. For developing hardware, obtaining installation experience,

and testing and validating the performance of the Super Cell readout, demonstrator boards have been built and installed in the ATLAS LAr Calorimeter and are being used at the current physics run. We have measured performance of the legacy readout and of the demonstrator readout. The results on the legacy system assure that the demonstrator system itself doesn't degrade the performance of energy measurement in the current physics run. The measurements of the prototype LTDB show that the prototype LTDB has an expected performance in terms of noise and linearity. The next targets with demonstrator system are to prepare a setup for taking data with *pp* collision at the 13 TeV physics run, to test new digital filtering algorithms for energy reconstruction.

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